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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,802	09/12/2003	Thomas D. Lovett	BEA920020019US1	8363

49474 7590 04/17/2008
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EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
04/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/661,802	LOVETT ET AL.	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on 1/9/2008, have been fully considered but are not persuasive. Applicant argues that the references relied upon do not teach the buffer also storing eviction data regarding the first memory line and data resulting from conversion of the second memory line into a set of concurrently performable actions. However, Williams, III discloses the buffer also storing eviction data regarding the first memory line (evicted data is written to the write buffer 14, paragraph 0036) and data resulting from conversion of the second memory line into a set of concurrently performable actions (set of performable actions that follow for the completion of a line fill operation, paragraphs 0042-0049).

Claim Objections

2. The Claim objection to Claim 1 is withdrawn in view of Applicant's Amendment.

Claim Rejections - 35 USC § 101

3. The rejection of Claims 20 under 35 U.S.C. 101 has been withdrawn in view of Applicant's Amendment.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1, 10, and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant points to the Specification, page 10 for support of the newly added limitation stating "the buffer also storing .... data resulting from conversion of the second memory line into a set of concurrently performable actions". The examiner does not see how this section of the specification, or any other section, appropriately supports this limitation.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1, 10, 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by converting the second memory line into a set of concurrently performable actions. It is also not understood how or when the second memory line is being moved from the buffer to the cache if it has been converted.

For the purpose of rejecting the claims, these claims will be interpreted as best understood by the examiner.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-5, 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Williams, III (2003/0110356 A1).

Regarding Claim 1, Williams III discloses a method comprising:

evicting a first memory line currently stored in a cache (cache data to replaced has been altered and must be written back to main memory 8, paragraph 0036) and storing a second memory line not currently stored in the cache in place of the first memory line in the cache (when the processor executes an instruction that causes a cache miss, a linefill operation retrieves data from the main memory, selects a victim cache line to replace with this data and writes the new data in the victim cache line, paragraph 0035);

while evicting the first memory line, temporarily storing the second memory line in a buffer (fill buffer 12); the buffer also storing eviction data regarding the first memory line (evicted data is written to the write buffer 14, paragraph 0036) and data resulting from conversion of the second memory line into a set of concurrently performable actions (set of performable actions that follow for the completion of a line fill operation, paragraphs 0042-0049);

upon eviction of the first memory line, moving the second memory line from the buffer into the cache (see paragraphs 0041-0049).

Regarding Claim 2, Williams III discloses the method further initially comprising receiving a transaction relating to the second memory line not currently in the cache (servicing write requests, paragraph 0041).

Regarding Claim 3, Williams III discloses the method further comprising, after temporarily storing the second memory line in the buffer, providing a response indicating that a transaction relating to the second memory line has been performed (wherein the response to the request is in the form of servicing the request, paragraph 0041).

Regarding Claim 4, Williams III discloses the method wherein evicting the first memory line currently stored in the cache comprises inserting the first memory line in an eviction queue of memory lines to be evicted from the cache (dirty data to be evicted is written out to a write buffer and then written to the main memory, paragraph 0036).

Regarding Claim 5, Williams III discloses the method wherein temporarily storing the second memory line in the buffer comprises temporarily storing the second memory line in a data transfer buffer (DTB). Dirty data to be evicted is written out to a write buffer wherein the write buffer is a DTB since it buffers that data that is being transferred from the cache to main memory (paragraph 0036).

Claim 18 is rejected using the same rationale as that of Claim 1 wherein the computer readable medium is main memory 8 (Figure 1) and the system is able to process transaction while a first memory line to which the transaction relates is being loaded into a cache (see paragraph 0041).

Regarding Claim 19, Williams III discloses the article wherein the means moves the first memory line from the buffer into the cache (when the processor executes an instruction that causes a cache miss, a linefill operation retrieves data from the main memory, selects a victim cache line to replace with this data and writes the new data in the victim cache line, paragraph

0035) after eviction of the second memory line from the cache (cache data to replaced has been altered and must be written back to main memory 8, paragraph 0036).

Regarding Claim 20, Williams III discloses the article wherein the medium is one of a recordable data storage medium (Main Memory 8, Figure 1).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams III (2003/0110356 A1) in view of Chryson et al. (6,549,930).

Regarding Claim 6, Williams III discloses the method of Claim 1 above. Williams III does not teach converting a transaction to which the second memory line relates into a set of concurrently performable actions using a multiple-stage pipeline. Chryson et al. discloses converting a transaction (in the pipeline the instructions are decoded for execution, Col. 8, lines 51-55) into a set of concurrently performable actions (plurality of stages serially arranged such as fetch, map, issue, execute, and retire, Col. 8, lines 62-64) using a multiple-stage pipeline (multiple execution pipeline, Col. 8, lines 34-36). It would have been obvious to one of ordinary skill in the art to modify the invention of Williams III to include the multiple stage pipeline of Chryson since the multiple stages of the pipeline allow improved system performance.

Regarding Claim 7, Williams III in view of Chryson et al. discloses the method wherein evicting the first memory line currently stored in the cache comprises inserting the first memory line in an eviction queue of memory lines to be evicted from the cache (dirty data to be evicted is written out to a write buffer and then written to the main memory, paragraph 0036) after the transaction has been converted into the set of concurrently performable actions (since a transaction causes the cache miss, which in turn caused the eviction, then the transaction must have been converted in order to be executed) .

Regarding Claim 8, Williams III discloses the method wherein temporarily storing the second memory line in the existing buffer comprises temporarily storing the second memory line in a data transfer buffer (DTB). Dirty data to be evicted is written out to a write buffer wherein the write buffer is a DTB since it buffers that data that is being transferred from the cache to main memory (paragraph 0036).

Regarding Claim 9, Williams III discloses the method further comprising, after temporarily storing the second memory line in the buffer, providing a response indicating that a transaction relating to the second memory line has been performed (wherein the response to the request is in the form of servicing the request, paragraph 0041).

12. Claims 10-14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams III (2003/0110356 A1) in view of Applicant's Admitted Prior Art (pages 1-3 of specification).

Regarding Claim 10, Williams III discloses a system comprising

a processor (core 4);

local random-access memory (RAM) for the processor (Main Memory 8, wherein the main memory may be a RAM, paragraph 0004); and,

at least one controller to manage transactions relative to the local RAM (controller 16 wherein this controller manages the eviction of dirty data to the RAM), the controller able to concurrently process the transactions while memory lines to which the transactions relate are being loaded into one or more caches by temporarily storing the memory lines into one or more buffers (processing transactions from the fill buffer, paragraph 0041); the one or more buffers also storing eviction data regarding memory lines to be evicted (evicted data is written to the write buffer 14, paragraph 0036) and data resulting from conversion of the memory lines into sets of concurrently performable actions (set of performable actions that follow for the completion of a line fill operation, paragraphs 0042-0049)

Williams III does not teach a plurality of processors. Applicant's Admitted Prior Art (AAPA) discloses a NUMA system wherein a plurality of processors share one common local memory (page 3, paragraph 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the system of Williams III in a NUMA environment as that of Applicant's Admitted Prior Art since NUMA is a multiprocessor system and therefore provides for processor redundancy in case of a processor failure.

Regarding Claim 11, Williams III in view of Applicant's Admitted Prior Art teaches the system wherein the local RAM is divided into a first memory bank and a second memory bank (memory is separated into distinct banks, AAPA), and the at least one controller comprises a first controller for managing transactions relative to the first memory bank, and a second controller

for managing transactions relative to the second memory bank (processors and banks from individual processing boards, page 3, paragraph 2).

Regarding Claim 12, Williams III in view of Applicant's Admitted Prior Art teaches the system further comprising a plurality of nodes (processing blocks), a first node including the plurality of processors, the local RAM, and the at least one controller, each other node also including a plurality of processors, local RAM, and at least one controller, the plurality of nodes forming a non-uniform memory access (NUMA) architecture in which each node is able to remotely access the local RAM of other of the plurality of nodes (see page 3, paragraph 2 of AAPA).

Regarding Claim 13, Williams III discloses the system wherein the one or more existing buffers comprise one or more data transfer buffers (DTBs). Dirty data to be evicted is written out to a write buffer wherein the write buffer is a DTB since it buffers that data that is being transferred from the cache to main memory (paragraph 0036).

Regarding Claim 14, Williams III discloses the system wherein each controller comprises an eviction queue into which other memory lines to be evicted from at least one of the one or more caches is inserted (dirty data to be evicted is written out to a write buffer and then written to the main memory, paragraph 0036).

Regarding Claim 17, Williams III discloses the system wherein the transactions comprise at least one of memory line-related requests (write request) and memory line-related responses (the response is in the form of servicing the request, paragraph 0041).

13. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams III (2003/0110356 A1) in view of Applicant's Admitted Prior Art and further in view of Chryson et al. (6,549,930).

Regarding Claim 15, Williams III in view of Applicant's Admitted Prior Art (AAPA) discloses the method of Claim 10 above. Williams III in view of Applicant's Admitted Prior Art does not teach converting a transaction to which the second memory line relates into a set of concurrently performable actions using a multiple-stage pipeline. Chryson et al. discloses converting a transaction (in the pipeline the instructions are decoded for execution, Col. 8, lines 51-55) into a set of concurrently performable actions (plurality of stages serially arranged such as fetch, map, issue, execute, and retire, Col. 8, lines 62-64) using a multiple-stage pipeline (multiple execution pipeline, Col. 8, lines 34-36). It would have been obvious to one of ordinary skill in the art to modify the invention of Williams III in view of Applicant's Admitted Prior Art to include the multiple stage pipeline of Chryson since the multiple stages of the pipeline allow improved system performance.

14. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams III (2003/0110356 A1) in view of Applicant's Admitted Prior Art and further in view of Scaringella et al. (5,890,219).

Regarding Claim 16, Williams III in view of Applicant's Admitted Prior Art discloses the system of claim 10 above. Williams III in view of Applicant's Admitted Prior Art does not teach each controller comprises an application-specific integrated circuit (ASIC). Scaringella et al. discloses a controller comprising an application-specific integrated circuit (ASIC, Col. 10, lines 22-48 and Col. 10, line 63-Col. 11, line 5). It would have been obvious to one of ordinary skill

in the art at the time the invention was made to implement the controller of Williams III in view of Applicant's Admitted Prior Art as an ASIC since these provide for a compact design, improved performance, and simpler integration with other components.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-TH 6:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Midys Rojas/
Examiner, Art Unit 2185

MR

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185